Debugging the core monitoring switch

Article Overview

Core monitoring can be achieved using monitor mode debugging, trace logging, and hardware/software co-debugging to observe CPU behavior without halting critical peripherals.

Monitor Mode Debugging

For ARM Cortex-M MCUs, monitor mode debugging allows you to debug the core without stopping time-critical operations. Unlike halt-mode debugging, which freezes the entire CPU, monitor mode triggers a DebugMonitor exception when a breakpoint or debug event occurs. The CPU executes a high-priority interrupt handler that communicates with the debugger while keeping critical peripherals, such as PWM or motor-control loops, running uninterrupted . This is particularly useful in production or real-time systems where halting the core could cause hardware faults or unsafe conditions. To enable monitor mode:

• Ensure halting debug is disabled by clearing the C_DEBUGEN bit in the core debug registers .
• Configure the DebugMonitor exception handler to service debug events, memory reads/writes, and step/run commands.
• Assign the handler a priority that allows it to run above background tasks but below critical ISRs to maintain system stability . Supported Cortex-M variants include M3, M4, M7, M23, M33, M55, and M85. Cortex-M0 and M0+ do not support monitor mode and require halt-mode debugging .

Trace-Based Core Monitoring...

Article Content

Chrome DevTools | Chrome for Developers

Monitor your local and real-user Core Web Vitals performance in DevTools Learn about new DevTools features like CPU throttling

Configure Remote Network Monitoring (RMON) Events Control

Article ID:5569 Configure Remote Network Monitoring (RMON) Events Control Settings on a Switch through the

Monitoring Routers and Switches · Nagios Core Documentation

Once you''ve added the new host and service definitions to the switch.cfg file, you''re ready to start monitoring the router/switch. To do

Debugger Tutorial

Welcome to this tutorial, designed to help you quickly get up and running with the TRACE32 hardware-assisted debugger. We''ll walk

[Check_mk (english)] Core Switch Monitoring

Hello, I''ve have an issue monitoring our core switches. There is so much information that comes back from an SNMP

WARNING: [Labtools 27-3361] The debug core was not detected

WARNING: [Labtools 27-3361] The debug hub core was not detected. Resolution: 1. Make sure the clock connected to

Development of a Core-Monitor for HW/SW Co-Debugging targetting ...

Core-Monitor is required to have a general HW/SW co-debugging environment for an embedded processor It generates a trace file

Top 8 Free Network Monitoring Software

Find out network monitoring benefits and the list of the top free and open-source automated monitoring solutions.

Switch Port Monitoring Guide

Learn how switch port monitoring enhances network performance, security, and troubleshooting. Explore top tools for

Open Hardware Monitor

The Open Hardware Monitor is a free open source software that monitors temperature sensors, fan speeds, voltages,

Cortex-M Debugger

The Cortex-M does not have a Debug Communication Channel (DCC) as other Cortex cores but even better it''s system memory can

Cisco Debug Command ⋆ | How to Use Cisco Debug Command?

With Cisco debug command, we display information about Cisco router & switch operations, activities or errors in real time. You can

Distributed Network Monitoring and Debugging with SwitchPointer

Abstract Monitoring and debugging large-scale networks remains a challenging problem. Existing solutions operate at one of the two

Learn the architecture

It also explains the debug system context for software development on Arm processors. Using the guide, you can learn how

Paper Title (use style: paper title)

This work aims to develop a Core-Monitor for Hardware-Software co-debugging targeting emulation platforms. Core-Monitor is

Lauterbach multicore debugging guide

Tools used are Lauterbach debugger and TRACE32 debugging interface. SPC56x families device combines DPM (decoupled) and

Catalyst 2960 Switch Debug Commands

This appendix describes the debug privileged EXEC commands that have been created or changed for use with the Catalyst 2960

Debugging of RISC-V-Based Chips Made Easy

Debugging of RISC-V-Based Chips Made Easy RISC-V cores can be found in increasingly more chips, either as the main CPU(s) or

Cortex-M Debug Monitor — Zephyr Project Documentation

Monitor mode debugging is a Cortex-M feature, that provides a non-halting approach to debugging. With this it''s

Inspecting, debugging, and profiling Core AI models

Investigate model behavior, monitor activity, and profile performance using the Core AI tools across Xcode and the Core AI

Monitoring System Processes and Logs

To view the time of the actual last core dump, enter the show process log command in EXEC mode. The first and last core feature

What is Switch Monitoring? Metrics, Tools & Best ...

What is switch monitoring? Learn what switch monitoring is, why it matters, and which metrics prevent outages.

Using kgdb, kdb and the kernel debugger internals

Using kgdb, kdb and the kernel debugger internals ¶ Author: Jason Wessel Introduction ¶ The kernel has two different debugger front

Setup of the Debugger for a CoreSight System

Introduction The Arm CoreSight technology provides additional debug and trace functionality with the objective of debugging an

Monitor Mode Debugging

The information in this post is outdated. Please refer this tutorial for updated information. Motivation Monitor Mode

ARMv8-A/-R Debugger

Once the boot core is stopped in debug mode, the secondary cores might still be in a power down or reset state. In this

ARMv8-A/-R Debugger

Enter Debug Mode 35 Switch Debug View between Cores 35 Write a Start-up Script Summary 35 AMP Debugging -

Monitoring System Processes and Logs

Monitoring System Processes and Logs This chapter provides details on monitoring the health of the switch and includes the

Mastering the challenges of multicore programming and debugging

Compared to the dual-core part, the diagram shown represents a much more complex chip to control. The C-SPY

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